

Applicant : Joerg-Erich Sorg et al.
Serial No. : 10/635,937
Filed : August 5, 2003
Page : 2

Attorney's Docket No. 12406-031001

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1-20. (Cancelled)

21. (Previously Presented) A method for producing a surface-mountable semiconductor component, comprising:

- a) applying an electrically insulating carrier layer (101) to an electrically conductive connection conductor layer (102), patterning at least one chip window (7) and at least one wire connection window (8) in the carrier layer (101), and patterning external electrical connection conductors (2,3) in the connection conductor layer (102);
- b) mounting a semiconductor chip (1) on a first side of one of the connection conductors (2) through the chip window (7), wherein the semiconductor chip is capable of emitting and/or receiving electromagnetic radiation;
- c) electrically connecting at least one electrical contact (5) of the semiconductor chip (1) to at least one of the connection conductors (3) by means of a bonding wire (50) through the wire connection window (8);
- d) placing the connection conductor layer (102), carrier layer (101), semiconductor chip (1) and bonding wire (50) into an injection mold; and
- e) encapsulating the semiconductor chip (1) and bonding wire (50) with an encapsulation material (6) by injection molding, wherein the encapsulation material is transparent, and subsequently at least partly or incipiently curing the material, wherein subsequent to the encapsulation step, the connection conductors (2,3) on a side opposite to the first side are exposed for electrical connection to an electrical component.

Applicant : Joerg-Erich Sorg et al.
Serial No. : 10/635,937
Filed : August 5, 2003
Page : 3

Attorney's Docket No. 12406-031001

22. (Previously Presented) The method as claimed in claim 21 wherein:

- in step a) producing an array (201) with a multiplicity of component regions (202), each component region (202) including at least one chip window (7), at least one wire connection window (8) and at least two external electrical connection conductors (2, 3);
- in steps b) and c), mounting a multiplicity of semiconductor chips (1) into a multiplicity of chip windows (7) and connecting an electrical contact (5) of each semiconductor chip (1) to one of the external electrical connections (3) by means of a bonding wire (50);
- in step d), placing the array into an injection mold (500), in which a single cavity (501) spans the multiplicity of component regions (202) of the array (201) and forms a void over the component regions exclusively on a side of the carrier layer on which the semiconductor chips are mounted; and
- in step e), introducing the encapsulation material (6) into the cavity (501) by injection molding and at least partly curing or incipiently curing the encapsulation material in the cavity; the method further comprising:
- removing the array (201) from the injection mold (500) and singulating the array into mutually separate semiconductor components by severing the encapsulation material (6) and the carrier layer (101).

23. (Previously Presented) A method for producing a surface-mountable semiconductor component, comprising:

- a) applying an electrically insulating carrier layer (101) to an electrically conductive connection conductor layer (102), patterning at least one chip window (7) in the carrier layer (101), and patterning external electrical connection conductors (2, 3) into the connection conductor layer (102), the connection conductors (2, 3) partly overlapping the chip window (7);
- b) mounting a semiconductor chip capable of emitting and/or receiving electromagnetic radiation onto the external electrical connection conductors (2, 3) in the chip window (7), in such a way that a first contact (4) and a second contact (5) of the semiconductor

Applicant : Joerg-Erich Sorg et al.
Serial No. : 10/635,937
Filed : August 5, 2003
Page : 4

Attorney's Docket No. 12406-031001

chip (1) are electrically connected to first sides of a first (2) and, respectively, a second (3) of the connection conductors;

c) placing the connection conductor layer (102), carrier layer (101) and semiconductor chip (1) into an injection mold (500); and

d) encapsulating the semiconductor chip (1) with a transparent encapsulation material (6) by injection molding, and subsequently at least partly or incipiently curing the material, wherein subsequent to the encapsulation step, sides opposite to the first sides of the connection conductors are exposed for electrical connection to an electrical component.

24. (Previously Presented) The method as claimed in claim 23, wherein:
in step a), producing an array (201) with a multiplicity of component regions (202), each component region (202) including at least one chip window (7) and at least two external electrical connection conductors (2, 3);

in step b), mounting a multiplicity of semiconductor chips (1) into a multiplicity of chip windows (7) and connecting the chips to the connection conductors (2, 3);

in step c), placing the array into an injection mold (500), in which a single cavity (501) spans the multiplicity of semiconductor chips (1) of the array (201) and forms a void over the semiconductor chips (1); and

in step d), introducing an encapsulation material (6) into the cavity (501) by injection molding and at least partly curing or incipiently curing the encapsulation material in the cavity; the method further comprising:

removing the array (201) from the injection mold (500) and singulating the array into mutually separate semiconductor components by severing the encapsulation material (6) and the carrier layer.

25. (Previously Presented) The method as claimed in either claim 21 or 23, in which the semiconductor chip (1) comprises a light-emitting diode chip.

Applicant : Joerg-Erich Sorg et al.
Serial No. : 10/635,937
Filed : August 5, 2003
Page : 5

Attorney's Docket No. 12406-031001

26. (Previously Presented) The method as claimed in claim 23, wherein mounting a semiconductor chip includes mounting a light-emitting diode chip having a light-generating epitaxial layer, in which the light-emitting diode chip is mounted onto the external electrical connection conductor in rotated fashion with the light-generating epitaxial layer facing toward said connection conductor.

27. (Original) The method as claimed in either claim 21 or 23, in which the carrier layer (101) consists essentially of a plastic film and the connection conductor layer (102) consists essentially of a metal film.

28. (Original) The method as claimed in claim 27, in which a thickness of the carrier layer (101) is less than 80 μm .

29. (Original) The method as claimed in claim 28, in which the thickness of the carrier layer is between from and including 30 μm and up to and including 60 μm .

30. (Original) The method as claimed in claims 27, in which a thickness of the connection conductor layer (102) is less than 80 μm .

31. (Original) The method as claimed in claim 30, in which thickness of the connection conductor layer (102) is between from and including 30 μm and up to and including 60 μm .

32. (Previously Presented) The method as claimed in claim 21, wherein the chip window (7) leads to a first of the connection conductors (2) and the wire connection window (8) leads to a second of the connection conductors (3), respectively.

Applicant : Joerg-Erich Sorg et al.
Serial No. : 10/635,937
Filed : August 5, 2003
Page : 6

Attorney's Docket No. 12406-031001

33. (Original) The method as claimed in either claim 21 or 23, in which the carrier layer (101) comprises a plastic layer that can be patterned by means of masking and etching techniques.

34. (Currently Amended) The method as claimed in [[a]] claim 33, in which a portion of the plastic layer (101) corresponding to at least the chip window (7) comprises an uncured and etchable plastic, and wherein the patterning step includes curing or incipiently curing the plastic layer except for a region (70) of the plastic layer corresponding to at least the chip window (7) and subsequently removing the region that was not cured or incipiently cured.

35. (Currently Amended) The method as claimed in claim 34, in which the patterning step includes applying a photoresist mask layer (103) to the plastic layer, patterning or applying the mask layer (103) in such a way that the region (70) of the plastic layer is covered by the mask layer (103), and exposing the plastic layer and mask layer to radiation so that the plastic layer except for the region covered by the mask layer is incipiently cured or cured.

36. (Previously Presented) The method as claimed in claim 34, in which the patterning step includes positioning a photomask (104) above or on said plastic layer, the photomask shading the region (70) of the plastic layer, exposing the plastic layer and photomask to radiation so that the plastic layer except for the region shaded by the photomask is cured or incipiently cured or cured, and lifting off the photomask (104).

37. (Currently Amended) The method as claimed in claim [[33]]34, in which the plastic layer is cured or incipiently cured by UV radiation (105).

38. (Currently Amended) The method as claimed in claim [[33]]34, in which the plastic layer is cured or incipiently cured by thermal radiation.

Applicant : Joerg-Erich Sorg et al.
Serial No. : 10/635,937
Filed : August 5, 2003
Page : 7

Attorney's Docket No. 12406-031001

39. (Currently Amended) The method as claimed in claim [[27]]33, in which the plastic layer includes a polyimide monomer.

40. (Currently Amended) The method as claimed in claim [[27]]34, in which removing the region that was not cured or incipiently cured includes etching the plastic layer.

41-45. (Cancelled)